REMARKS

Claims 1-4, 6, 9-27, and 31-35 are pending, with claims 1, 12, and 23 being in independent form. By the present amendment, claims 1, 6, 10, 21, 23, 31, and 33 have been amended, and claims 5, 7, 8, and 28-30 have been canceled without prejudice or disclaimer.

In the Office Action, claims 10, 20, and 33 stand rejected for indefiniteness. Although the Office cites claim 20 in the rejection, it is believed that the rejection is directed to claim 21. To address the Office's concern, the Applicants have amended claims 10, 21, and 33 to make more clear that the high-resistant substrate is etched to expose a portion of the bottom of the first compound semiconductor layer that is larger than a portion of the first compound semiconductor layer that remains in contact with the high-resistant substrate after etching. Support for the amendment may be found throughout the application, and in particular in the last sentence of paragraph [0094] on page 27 of the specification. Accordingly, the Applicants respectfully request that the Office reconsider and withdraw the indefiniteness rejection with respect to claims 10, 21 (cited as claim 20 in the Action), and 33.

The Office Action also includes a rejection asserting that the term "high-shielding" renders claim 1 indefinite. The Applicants have amended the claim to replace the objected-to term with the term "light-shielding". Support for the Amendment may be found throughout the application, and in particular in the last sentence of paragraph [0047] on page 13 of the specification. Accordingly, the Applicants respectfully request that the Office reconsider and withdraw the indefiniteness rejection of claim 1 for this reason as well.

The Office Action includes another rejection asserting that the recitation of "high-resistant substrate" in the claims renders the claims indefinite. The Applicants respectfully disagree for the following reasons.

According to MPEP § 1703.05(b), the fact that claim language, including terms of degree, may not be precise, does not automatically render the claim indefinite under 35 U.S.C. 112, second paragraph. *Citing, Seattle Box Co., v. Industrial Crating& Packing, Inc.*, 731 F.2d 818, 221 U.S.P.Q. 568 (Fed. Cir. 1984). Instead, the test is whether one of ordinary skill in the art would understand what is claimed, in light of the specification, or whether one of ordinary skill in the art, in view

of the prior art and the status of the art, would be nevertheless reasonably apprised of the scope of the invention.

The Applicants believe that a person of ordinary skill in the semiconductor arts would understand from both the specification and the state of the art at the time of the invention that the scope of the term high-resistant substrate includes substrates comprised of materials through which an electrical contact is not generally made under normal operating conditions. For example, the Applicants describe near the end of paragraph [0015], bridging pages 4 and 5 of the specification, that a light-emitting diode (LED) fabricated according to embodiments of the invention includes a high-resistant substrate formed on the bottom of the first compound semiconductor layer while being partially removed to allow an electrical contact between the first compound semiconductor layer and the first electrode.

The Applicants also describe in the Background section that conventional LEDs based on gallium nitride (GaN) based III-V nitrides can include an n-type GaN layer 12 on a sapphire substrate 10, and that an n-type electrode 14 can be formed in the second region R2 of the n-type GaN layer 12 to contact the n-type layer. *See*, p. [0004], and FIG. 1. The Applicants further describe in the Background section that conventional GaN based III-V nitride semiconductor laser diodes having an n-type GaN layer 12 can also be formed on a silicon carbide (SiC) substrate 10a (or a GaN substrate), and that an n-type electrode 14a can be formed on the bottom of the SiC or GaN substrate 10a to contact the n-type GaN layer 12. *See*, p. [0007], pg. 3, and FIG. 3.

The Applicants further describe, in conjunction with FIG. 9, on page 13, paragraph [0050] of the specification, that a first compound semiconductor layer 152 can be formed on a substrate 150, and that the substrate 150 can be a high-resistant substrate, such as a sapphire substrate, or a III-V compound semiconductor such as a GaN or silicon carbide (SiC) substrate.

For the foregoing reasons, it is believed that sufficient guidance as to the meaning of the relative term "high" in the recited phrase "high-resistant substrate" is provided in the original specification. Accordingly, the Applicants respectfully request that the Office reconsider and withdraw this indefiniteness rejection as well.

Turning to the art rejections, claims 1-3, 9-15, 20-27, and 32-35 stand rejected for anticipation by U.S. Patent No. 6,468,902 to Kawai. In addition, Claims 5-8, 16-19, and 28-31 are rejected for obviousness over Kawai in view of U.S. Patent No. 5,905,275 to Nunoue et al. ("Nunoue"). Although claim 4 is not specifically referenced by number in the Action, the Applicants acknowledge that the Office asserts on page 3 of the Action that the claim reads on Kawai. Nevertheless, the Applicants respectfully assert that the pending claims are allowable over the cited documents for the following reasons.

Claims 1 and 23 have been amended to incorporate the features of dependent claims 5 and 28, respectively. The amendment renders moot the anticipation rejection of claims 1 and 23. Consequently, the Applicants will address the obviousness rejection of claims 5 and 28 in arguing for the patentability of amended claims 1 and 23.

In accordance with the MPEP, three criteria must be met to establish a prima facie case of obviousness. First, the cited documents must describe or suggest all of the claim features. Second, there must be some suggestion or motivation, either in the cited documents themselves or in the knowledge generally available to one of ordinary skill in the art, to have combined the teachings of the cited documents. Third, there must have been a reasonable expectation that the documents could have been successfully combined to yield the claimed invention.

The obviousness rejection raised in the Action should not stand because, as admitted in the Action, Kawai does not describe "dry etching a region of the high-resistant substrate using a reaction gas comprising at least Cl_2 or BCl_3 to expose the first compound semiconductor layer". Thus, the required motivation to combine Kawai with any document, much less Nunoue, to prove the prima facie case is lacking.

For example, Kawai states at col. 2, ll. 37-44, that:

> Also regarding the via hole to be made in the sapphire substrate, since sapphire is very stable in chemical property, wet etching cannot be used without any effective etchant. As to dry etching by RIE, since its etching rate is as very low as several μm/hr in maximum, and there is no etching mask having a selectivity acceptable for selective etching. Therefore, it is actually impossible to make the via hole with any of these methods. (emphasis added)

Kawai further states at col. 4, ll. 52-53, that "[f]or making the via hole, dry etching such as conventional RIE cannot be employed".

Such strong and unambiguous language would discourage persons skilled in the art at the time of the invention to combine Kawai with any document, including Nunoue, that advocates dry etching a region of the high-resistant substrate, such as sapphire, as recited in claims 1 and 23.

In addition to strongly discouraging the use of a dry-etch process to form its via hole, Kawai describes in detail a wet-etch process in which the bottom surface side of a sapphire substrate 1 is immersed into an etchant of phosphoric/sulfuric acid solution held at approximately 280°C. Although Kawai describes that a dry-etch RIE process can be used to etch part of the GaN semiconductor layer 2 exposed at the bottom of the via hole 8 previously removed by the wet-etch process, it is clear from the document that the sapphire substrate 1 is not etched using the dry-etch RIE process. *See*, col. 5, ll. 8-10 and 15-17. Moreover, Kawai describes in conjunction with the embodiment shown in FIG. 14, that "using the same [wet-etch] method as used in the first and second embodiments, the via hole 61 is made by selecting (sic) removing a part of the c-plane sapphire substrate in alignment with the p-side electrode 60 from the bottom thereof". Col. 13, ll. 37-41.

Accordingly, claims 1 and 23, as amended, are considered allowable over the combination of Kawai and Nunoue because neither of the documents alone describe or suggest all of the claimed features, and because the requisite motivation to combine the cited documents is lacking. The claims that depend from either claim 1 or claim 23 are considered to be allowable for at least these same reasons.

Regarding the rejection of claim 12, anticipation requires that every feature of the claimed invention be shown in a single prior document. *In re Paulsen*, 30 F.3d 1475 (Fed. Cir. 1994); *In re Robertson*, 169 F.3d 743 (Fed. Cir. 1999). Claim 12 positively recites features that are not described in Kawai.

For example, claim 12 recites, among other things, "sequentially forming a first compound semiconductor layer, an active layer, and a second compound semiconductor layer, which are for inducing light emission, on a high-resistant substrate", "etching a region of the high-resistant substrate to expose the first compound semiconductor layer", and "forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer". Accordingly,

the first compound semiconductor layer is arranged on the high-resistant substrate, and a light-transmitting conductive layer is formed to cover a region of the first compound semiconductor layer exposed through a corresponding exposed region of the high-resistant substrate. Kawai does not describe these features.

The first compound semiconductor recited in claim 12 can read only on the exposed regions of Kawai's GaN semiconductor layer 22 shown in FIG. 11 and the GaN buffer/contact layer 52/53 shown in FIG. 14. Kawai describes that the conductive layer 36/37 covering the exposed region of GaN semiconductor layer 22 in FIG. 11 consists of chromium (Cr) and gold (Au). Persons skilled in the art would understand that these metal layers are not light-transmitting as the claim recites, but instead are light-reflecting layers. The Office admits as much on page 3 of the Action. Likewise, Kawai describes that the conductive layer 62 covering the exposed region of the GaN buffer/contact layer 52/53 shown in FIG. 14 consists of titanium (Ti) and aluminum (Al), which are also not light-transmitting layers.

Accordingly, the Applicants respectfully assert that claim 12 is allowable over Kawai at least because the cited document does not describe forming a light-transmitting conductive layer to cover the exposed region of the first compound semiconductor layer. Moreover, dependent claims 13-22 are considerable allowable for at least this same reason.

It is believed this application is in condition for allowance and an early Notice thereof is earnestly solicited. If any questions remain, the Examiner is invited to phone the undersigned at the below-listed number.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Stephen J. Lytran
Registration No. 45,846

P.O. Box 1404
Alexandria, Virginia 22313-1404
(919) 941-9240

Date: 6/17/2004

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Kathryn L. Boyd Date June 17, 2004